Question # 1 of 30 (Start time: 06:45:40 PM, 27 December 2020)

In SRC, the op-code for NOP operation is _____.

Select the correct option

- [x] 0
- [ ] 2
- [ ] 3
- [ ] 6

Question # 2 of 30 (Start time: 06:45:58 PM, 27 December 2020)

_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

Select the correct option

- INC4
- LPC
- PCout
- LC

Question # 4 of 30 (Start time: 06:48:39 PM, 27 December 2020)

In which of the following addressing modes, the address of the memory from where the value is to be accessed is given in the instruction?

Select the correct option

- (●) Direct Addressing
- ( ) Immediate Addressing
- ( ) Indirect Addressing
- ( ) Register Direct Addressing

Question # 5 of 30 (Start time: 06:50:08 PM, 27 December 2020)

The instruction fetch procedure generally takes _____ time step(s).

Select the correct option

- one
- two
- three
- four

Question # 6 of 30 (Start time: 06:51:33 PM, 27 December 2020)

To connect together N registers in a point to point scheme, we require _____ connections.

Select the correct option

- N(N+1)
- N(N-1)
- 2N
- 2N(N-1)

Question # 7 of 30 (Start time: 06:52:36 PM, 27 December 2020)

Which one of the following registers holds the instruction that is being executed?

Select the correct option

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

Question # 8 of 30 (Start time: 06:53:43 PM, 27 December 2020)

The MAR is connected directly to the _____.

Select the correct option

- MBR
- CPU internal bus
- CPU external bus
- LIC

Click to Save Answer & Move to

Question # 9 of 30 (Start time: 06:55:00 PM, 27 December 2020)

The control signal LIR allows the IR (Instruction Register) to read the instruction which is initially stored in _____ register.

Select the correct option

- MAR
- PC
- MBR
- Register A

Question # 10 of 30 (Start time: 06:56:26 PM, 27 December 2020)

The_____ control signal enables the input to the register C for writing the incremented value of PC onto it.

Select the correct option

- INC4
- LC
- PCout
- LPC

Question # 11 of 30 (Start time: 06:57:11 PM, 27 December 2020)

The Memory Buffer Register (MBR) has a _____ connection with both the memory sub-system and the registers/ALSU.

Select the correct option

- zero-directional
- uni-directional
- bi-directional
- tri-directional

Question # 12 of 30 (Start time: 06:58:12 PM, 27 December 2020)

Which type of Instruction is stored in instruction register (IR)?

Select the correct option

- (●) Current instruction being executed
- ( ) Next instruction to be executed
- ( ) Previously executed instruction
- ( ) Next branch instruction in the instruction sequence

Question # 13 of 30 (Start time: 06:58:55 PM, 27 December 2020)

A Stack based machine is also called _____.

Select the correct option

- 0-address machine
- 1-address machine
- 2-address machine
- 3-address machine

Question # 14 of 30 (Start time: 06:59:26 PM, 27 December 2020)

The third stage of the Pipelined version of SRC is;

Select the correct option

- ○ Instruction Fetch
- ● ALU operation
- ○ Memory access
- ○ Register write

Question # 15 of 30 (Start time: 07:00:07 PM, 27 December 2020)

A _____ is a computer program used to aid in detecting errors in a program.

Select the correct option

- (●) Debugger
- ( ) Assembler
- ( ) Linker
- ( ) Compiler

Question # 16 of 30 (Start time: 07:00:46 PM, 27 December 2020)

What functionality is performed by the instruction "str R8, 34" of SRC?

Select the correct option

- It will load the register R8 with the contents of the memory location M [PC+34]
- It will load the register R8 with the contents of the memory location M [34]
- It will store the register R8 contents to the memory location M [PC+34]
- It will store the register R8 contents to the memory location M [34]

Question # 17 of 30 (Start time: 07:02:00 PM, 27 December 2020)

_____ form the branch control field in the micro instruction.

Select the correct option

- C Bits
- M Bits
- B Bits
- A Bits

Question # 18 of 30 (Start time: 07:02:57 PM, 27 December 2020)

In a simple RISC computer, the size of each register is _____.

Select the correct option

- 16 bits
- 24 bits
- 32 bits
- 64 bits

Question # 19 of 30 (Start time: 07:03:19 PM, 27 December 2020)

A _____ processor is based on a very long instruction word.

Select the correct option

- [x] VLIW
- [ ] SRC
- [ ] FALCON-A
- [ ] FALCON-E

Question # 20 of 30 (Start time: 07:03:37 PM, 27 December 2020)

The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by _____.

Select the correct option

- Data forwarding
- Data compressing
- Instruction forwarding
- Instruction handling

Question # 21 of 30 (Start time: 07:04:26 PM, 27 December 2020)

MC68000 has a 32-bit program counter but only the least significant _____ bits are used.

Select the correct option

- 8
- 16
- 20
- 24

Question # 22 of 30 (Start time: 07:06:03 PM, 27 December 2020)

Control signal for RTL "IR <-- MBR" will be_____

Select the correct option

- (●) MBRout, LIR
- ( ) PC <-- C
- ( ) PC<--MBR
- ( ) PC<--IR

Question # 23 of 30 (Start time: 07:07:09 PM, 27 December 2020)

_____ form the branch address field in the micro instruction.

Select the correct option

- C Bits
- M Bits
- B Bits
- A Bits

Question # 25 of 30 (Start time: 07:09:12 PM, 27 December 2020)

Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Select the correct option

- (●) Arithmetic
- ( ) Control
- ( ) Data transfer
- ( ) Floating point

Question # 26 of 30 (Start time: 07:10:47 PM, 27 December 2020)

In "Jump [8]" instruction, the size of the constant field is _____ bits.

Select the correct option

- 4
- 5
- 8
- 16

Question # 27 of 30 (Start time: 07:12:33 PM, 27 December 2020)

In Structural RTL, the first three time steps (i.e. T0, T1 and T2) are of the instruction _____ phase.

Select the correct option

- (●) fetch
- ( ) execute
- ( ) create
- ( ) destroy

Question # 28 of 30 (Start time: 07:13:26 PM, 27 December 2020)

In FALCON A Program Counter (PC) and Instruction Register (IR) are of _____ bits

Select the correct option

- 16-bits
- 24-bits
- 32-bits
- 64-bits

Question # 29 of 30 (Start time: 07:13:58 PM, 27 December 2020)

The RTL description "IO[32] ← R[5]" represents which of the following instructions of EAGLE?

Select the correct option

- out 32, r5
- in 32, r5
- ori 32, r5
- mov 32, r5

Question # 30 of 30 (Start time: 07:15:44 PM, 27 December 2020)

In Falcon-A ISA, which of the following opcodes is used to perform "No Operation"?

Select the correct option

- 20
- 21
- 22
- 23

Click to Save Answer & Move to