

CS302 Short Notes

- ⇒ ABEL : Advanced Boolean Expression Language; a software compiler language for SPLD programming; a type of hardware description language (HDL)
- ⇒ Adder : A digital circuit which forms the sum and carry of two or more numbers.
- ⇒ address : The location of a given storage cell or group of cells in a memory; a unique memory location containing one byte.
- ⇒ address bus : Generally, a one-way group of conductors from the microprocessor to memory, containing the address information.
- ⇒ Analog : A signal which is continuously variable and, unlike a digital signal, does not have discrete levels. (A slide rule is analog in function.)
- ⇒ Analog Computer : Computer which represents numerical quantities as electrical and physical variables. Solutions to mathematical problems are accomplished by manipulating these variables.
- ⇒ AND Gate : A basic logic gate that outputs a 1 only if both inputs are a 1 , otherwise outputs a 0. See also, NAND, NOR and OR.
- ⇒ BCD : See 'Binary Coded Decimal'.
- ⇒ Binary : The binary number system has only two digits - 0 and 1.
- ⇒ Binary Code : A code in which each element may be either of two distinct values (eg the presence or absence of a pulse).
- ⇒ Binary Coded Decimal : A coding system in which each decimal digit from 0 to 9 is represented by four bits.
- ⇒ Bit : A single digit of a binary number. A bit is either a one represented by a voltage or a zero represented by no voltage. The number 5 represented in 4 and 8 bit binary would be 0101 and 00000101 respectively.
- ⇒ Boolean Algebra : The algebra of logic named for George Boole. Similar in form to ordinary algebra, but with classes, propositions, yes/no criteria, etc for variables rather than numeric quantities. It includes the operators AND, OR, NOT, IF, EXCEPT, THEN.
- ⇒ cascade : To connect 'end-to-end' as when several counters are connected from the terminal count output of one counter to the enable input of the next

counter.

- ⇒ Clock : The device in a digital system which provides the continuous train of pulses used to synchronize the transfer of data. Sometimes referred to as "the heartbeat."
- ⇒ CMOS : (Complementary Metal Oxide Semiconductor) An advanced IC manufacturing process technology characterized by high integration, low cost, low power and high performance. CMOS is the preferred process for today's high density ICs.
- ⇒ Combinational Logic : Logic circuits whose outputs depend only on the present logic inputs.
- ⇒ comparator : A digital circuit that compares the magnitudes of two quantities and produces an output indicating the relationship of the quantities.
- ⇒ counter : A digital circuit capable of counting electronic events, such as pulses, by progressing through a sequence of binary states.
- ⇒ data selector : A circuit that selects data from several inputs one at a sequence and places them on the output: also called a multiplexer.
- ⇒ Decoder : A logic function that uses a binary value, or address, to select between a number of outputs and to assert the selected output by placing it in its active state.
- ⇒ Digital System : A system in which information is transmitted in a series of pulses. The source is periodically sampled, analyzed, and converted or coded into numerical values and transmitted. Digital transmissions typically use the binary coding used by computers so most data is in appropriate form, but verbal and visual communication must be converted. Many satellite transmissions use digital formats because noise will not interfere with the quality of the end product, producing clear and higher-resolution imagery.
- ⇒ emitter : One of the three regions in a bipolar junction transistor.
- ⇒ encoder : A digital circuit(device) that converts information to a coded form.
- ⇒ even parity : The condition of having an even number of 1s in every group of bits.
- ⇒ exponent : The part of floating point number that represents the number of places that the decimal point (or binary point) is to be moved.
- ⇒ fan in : The number of logic inputs into a logic gate.

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- ⇒ fan out : The number of logic inputs that can be driven by the output of a logic gate.
- ⇒ flip-flop : A basic digital building block that, at its simplest, uses two gates cross-coupled so that the output of one gate serves as the input of the other. It is capable of changing from one state to another on application of a control signal, but can remain in that state after the signal is removed. It thus serves as a basic storage element. Most flip-flops contain additional features to make them more versatile. Many digital circuits, such as registers and counters, are a number of flipflops connected together.
- ⇒ GAL : Generic array logic; an SPLD with a reprogrammable AND array, a fixed OR array, and programmable output logic macrocells.
- ⇒ Gate : The control terminal of a MOSFET, or alternately a basic digital logic element, for example an AND Gate, See also, OR, NAND, NOR.
- ⇒ Gate Array : An integrated circuit made up of digital logic gates that are not yet connected. Typically gate arrays are fabricated up to the metal layers and then a custom metal mask is designed for a customer and used to connect the gates into a customer specific circuit.
- ⇒ Gray code : The mirror image of the binary counting code which changes one bit at a time when increasing or decreasing by one.
- ⇒ half-adder : A digital circuit that adds two bits and produces a sum and output carry. It cannot handle input carries.
- ⇒ High : A digital logic state corresponding to a binary "1."
- ⇒ High logic : In digital logic, the more positive of the two logic levels in a binary system. Normally, a high logic level is used to represent a binary 1 or true condition.
- ⇒ IC : (Integrated Circuit) A single piece of silicon on which thousands or millions of transistors are combined. ICs are the major building blocks of modern electronic systems.
- ⇒ Inverter : In logic, a digital circuit which inverts the input signal, as for example, changing a 1 to a 0. This is equivalent logically to the NOT function. An inverter may also serve as a buffer amplifier.
- ⇒ JK flip-flop : A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes.
- ⇒ Karnaugh map : An arrangement of cells representing the combinations of

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literals in a Boolean expression and used for a systematic simplification of the expression.

- ⇒ latch : A bistable digital circuit used for storing a bit.
- ⇒ LED : Light-Emitting Diode (component) Abbreviated LED. A semiconductor diode, generally made from gallium arsenide, that can serve as an infrared or visible light source when voltage is applied continuously or in pulses.
- ⇒ Logic : One of the three major classes of ICs in most digital electronic systems: microprocessors, memory, and logic. Logic is used for data manipulation and control functions that require higher speed than a microprocessor can provide
- ⇒ Low : A logic state corresponding to a binary "0". Satellite imagery is displayed on a computer monitor by a combination of highs and lows.
- ⇒ Low logic : In digital logic, the more negative of the two logic levels in a binary system. In positive logic, a low-logic level is used to represent a logic 0, or a not-true, condition.
- ⇒ mantissa : The magnitude of a floating-point number.
- ⇒ MSI : Medium-scale integration' a level of fixed-function IC complexity in which there are 12 to 99 equivalent gates per chip.
- ⇒ Multiplexer : An electronic device normally used to scan a number of input terminals and receive data from, or send data to, the same. Multiplexers are normally one of two types:
 - ⇒ The cyclic type which continually and sequentially looks at each input for a request to send or receive data.
 - ⇒ The random type which waits in a "rest" position until other circuitry notifies it of a request to receive or send data.
- ⇒ NAND gate : A logic circuit in which a LOW output occurs only if all the inputs are HIGH.
- ⇒ NOR gate : A logic circuit which performs the OR function and then inverts the result. A NOT-OR gate.
- ⇒ NOT : The logical operator having that property which if P is a statement, then the not of P (P) is true if P is false, and the not of P (P) is false if P is true.
- ⇒ octal : Describes a number system with a base of eight.
- ⇒ odd parity : The condition of having an odd number of 1s in every group of bits.

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- ⇒ OR gate : A multiple-input gate circuit whose output is energized when any one or more of the inputs is in a prescribed state. Used in digital logic
- ⇒ overflow : The condition that occurs when the number of bits in a sum exceeds the number of bits in each of the numbers added.
- ⇒ PAL : Programmable array logic; an SPLD with a programmable AND array and a fixed OR array with programmable output logic.
- ⇒ parity : In relation to binary codes, the condition of evenness or oddness of the number of 1s in a code group.
- ⇒ parity bit : A bit attached to each group of information bits to make the total number of 1s in a code group.
- ⇒ PLA : Programmable logic array; an SPLD with programmable AND and OR arrays.
- ⇒ queue : A high-speed memory that stores instructions or data.
- ⇒ register : A digital circuit capable of storing and shifting binary information; typically used as a temporary storage device.
- ⇒ Shift : To move information serially right or left in a register(s). Information shifted out of a register may be lost, or it may be re-entered at the other end of the register.
- ⇒ Shift register : A shift register is an electronic device which can contain several bits of information. Shift registers are normally used to collect variable input data and send this data out in a predetermined pattern.
- ⇒ Sign bit : Computers generally indicate whether a number is positive or negative by a sign bit, which is usually located adjacent to the most significant numerical digit. Usually zero (0) is used for positive (+) and one (1) for negative (-).
- ⇒ Significant digit : A digit that contributes to the preciseness of a number. The number of significant digits is counted beginning with the digit contributing the most value, called the most significant digit, and ending with the one contributing the least value, called the least significant digit.
- ⇒ toggle : The action of flip-flop when it changes state on each clock pulse.
- ⇒ Truth Table : A table that defines a logic function by listing all combinations of input values, and indicating for each combination the true output values.
- ⇒ TTL : Transistor-transistor logic; a class of integrated logic circuits that uses

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bipolar junction transistors.

- ⇒ universal gate : Either a NAND or a NOR gate; The term universal refers to the property of a gate that permits any logic function to be implemented by that gate or by a combination of gates of that kind.
- ⇒ up/down counter : A counter that can progress in either direction through a certain sequence.
- ⇒ VLSI : Very large-scale integration; a level of IC complexity in which there are 10,000 to 99,000 equivalent gates per chip.
- ⇒ volatile : A term that describes a memory that loses stored data when the power is removed.
- ⇒ weight : The value of digit in a number based on its position in the number.

****QUESTION:** For BCD numbers that add up to an invalid BCD number or generate a carry the number 6 (0110) is added to the invalid number, why ?

****ANSWER:** These binary numbers are not allowed in the BCD code: 1010, 1011, 1100, 1101, 1110, 1111

Then, if the addition produces a carry and/or creates an invalid BCD number, an adjustment is required to correct the sum. The correction method is to add 6 to the sum in any digit position that has caused an error. The correction method is to add 6 to the sum in any digit position that has caused an error.

For example,

$$15 + 9 = 24$$

$$0001\ 0101 = 15$$

$$+ 0000\ 1001 = 9$$

$$0001\ 1110 = 1? \text{ (invalid 1110)}$$

$$0001\ 1110 = 1? \text{ (invalid)}$$

$$+ 0000\ 0110 = 6 \text{ (adjustment)}$$

$$0010\ 0100 = 24$$

****QUESTION:** Why do we use +0V and +5V instead of +0V and +1V in DLD, when it is always '0' and '1' ?

****ANSWER:** In DLD, the circuits of logic gates (embedded in IC's) are operated with +5 Volts input. That is why we refer to +5 V for these logic inputs. It is considered as binary 1 when the +5V are applied to the logic gate, and binary 0 when 0 V are applied to the logic gate.

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****QUESTION:** What is the difference between asynchronous and synchronous counters?

****ANSWER:** Synchronous refers to the situation when all the interrelated devices has some common and fixed time relationship. Whereas in Asynchronous refers to the situation when the situation is opposite.
In Synchronous counters all the flip-flops have same clock pulse and in Asynchronous counters flip-flops does not change state at the exactly same time because they don't have common clock pulse.

****QUESTION:** What is meant by D in gated D latch and what is the function of this D input. What is the basic difference between latches and flip-flops?

****ANSWER:** The 'D' in 'Gated D Latch' stands for 'Data'.

Unlike 'S-R Latch' Gated D Latch has only one input, which is D(data) Input. Which will give the output of the latch depending on the 'EN' (enable) state of the latch.

To understand latches and flip-flops let's consider a basic fact about the whole DLD. In the same way that gates are the building blocks of combinatorial circuits, latches and flip-flops are the building blocks of sequential circuits. While gates had to be built directly from transistors, latches can be built from gates, and flip-flops can be built from latches.

Both latches and flip-flops are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs. The difference between a latch and a flip-flop is that

a latch does not have a clock signal, whereas a flip-flop always does

Latches are asynchronous, which means that the output changes very soon after the input changes. A flip-flop is a synchronous version of the latch.

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****QUESTION:** I cannot understand the timing diagram for the master slave flip flop.

****ANSWER:** A master-slave flip-flop is constructed from two separate flip-flops. One circuit serves as a master and the other as a slave. The logic diagram of an SR flip-flop is shown here. The master flip-flop is enabled on the positive edge of the clock pulse CP and the slave flip-flop is disabled by the inverter. The information at the external R and S inputs is transmitted to the master flip-flop. When the pulse returns to 0, the master flip-flop is disabled and the slave flip-flop is enabled. The slave flip-flop then goes to the same state as the master flip-flop.

Logic diagram of a master-slave flip-flop

The timing relationship is also shown here and is assumed that the flip-flop is in the clear state prior to the occurrence of the clock pulse. The output state of the master-slave flip-flop occurs on the negative transition of the clock pulse. Some master-slave flip-flops change output state on the positive transition of the clock pulse by having an additional inverter between the CP terminal and the input of the master.

Timing relationship in a master slave flip-flop.

****QUESTION:** I am not able to understand the truth table and timing diagram of " S-R Edge-triggered flip-flop, D edge-triggered flip-flop and J-K edge-triggered flip-flop kindly explain it in detail.

****ANSWER:** An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are called asynchronous inputs, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, these asynchronous inputs must both be kept LOW.

The basic operation of Edge-triggered S-R flip-flop is illustrated below, along with the truth table for this type of flip-flop. The operation and truth table for a negative edge-triggered flip-flop are the same as those for a positive except that the falling edge of the clock pulse is the triggering edge.

Note that the S and R inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output. This is illustrated in the timing diagram below:

While an Edge-triggered J-K flip-flop works very similar to S-R flip-flop. The only difference is that this flip-flop has NO invalid state. The outputs toggle (change to the opposite state) when both J and K inputs are HIGH. The truth table is shown below.

The operations of an Edge-triggered D flip-flop is much more simpler. It has only one input addition to the clock. It is very useful when a single data bit (0 or 1) is to be stored.

If there is a HIGH on the D input when a clock pulse is applied, the flip-flop SETs and stores a 1. If there is a LOW on the D input when a clock pulse is applied, the flip-flop RESETs and stores a 0. The truth table below summarizes the operations of the positive edge-triggered D flip-flop. As before, the negative edge-triggered flip-flop works the same except that the falling edge of the clock pulse is the triggering edge.

****QUESTION:** What is Multiplexer and what are its applications and expression simplification using Multiplexer?

****ANSWER:** Multiplexer is a digital circuit with multiple signal inputs, one of which is selected by separate address inputs to be sent to the single output. The multiplexer circuit is typically used to combine two or more digital signals onto a single line, by placing them there at different times. Technically, this is known as time-division multiplexing.

Input A is the addressing input, which controls which of the two data inputs, X0 or X1, will be transmitted to the output. If the A input switches back and forth at a frequency more than double the frequency of either digital signal, both signals will be accurately reproduced, and can be separated again by a demultiplexer circuit synchronized to the multiplexer.

This is not as difficult as it may seem at first glance; the telephone network combines multiple audio signals onto a single pair of wires using exactly this technique, and is readily able to separate many telephone conversations so that everyone's voice goes only to the intended recipient. With the growth of the Internet and the World Wide Web, most people have heard about T1 telephone lines. A T1 line can transmit up to 24 individual telephone conversations by multiplexing them in this manner.

A very common application for this type of circuit is found in computers, where dynamic memory uses the same address lines for both row and column addressing. A set of multiplexers is used to first select the row address to the memory, then switch to the column address. This scheme allows large amounts of memory to be incorporated into the computer while limiting the number of copper traces required to connect that memory to the rest of the computer circuitry. In such an application, this circuit is commonly called a data selector. Multiplexers are not limited to two data inputs. If we use two addressing inputs, we can multiplex up to four data signals. With three addressing inputs, we can multiplex eight signals.

****QUESTION:** What is an equivalent representation for the Boolean expression $A' + 1$?

****ANSWER:** From the Boolean property $A + 1 = 1$, let $A = A'$.

****QUESTION:** What is K-map and why we used it?

****ANSWER:** A Karnaugh map provides a pictorial method of grouping together expressions with common factors and therefore eliminating unwanted variables. The Karnaugh map can also be described as a special arrangement of a truth table.

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****QUESTION:** Each stage in a shift register represents how much storage capacity?

****ANSWER:** one bit

****QUESTION:** How can a D flip-flop can be made to toggle?

****ANSWER:** A D flip-flop can be made to toggle by connecting Q' to D.

****QUESTION:** What is the difference between a counter and shift register ?

****ANSWER:** A counter has a specified sequence of states, but a shift register does not.

****QUESTION:** What is BCD and how do we write them?

****ANSWER:** BCD (Binary-Coded Decimal) is a system for encoding Decimal Numbers in binary form to avoid rounding and conversion errors. In BCD coding, each digit of a decimal number is coded separately as a binary numeral. Each of the decimal digits 0 through 9 is coded in four bits, and for ease of reading, each group of four bits is separated by a space. This format, also called 8-4-2-1 after the weights of the four bit positions, uses the following codes:

0000 = 0

0001 = 1

0010 = 2

0011 = 3

0100 = 4

0101 = 5

0110 = 6

0111 = 7

1000 = 8

1001 = 9

Thus, the decimal number 12 is 0001 0010 in binary-coded decimal notation.

****QUESTION:** Where do we use Caveman Number System ?

****ANSWER:** Caveman Number System was introduced in old ages as symbolic representation of decimal number system. You do not need to study it in detail, as it is also mentioned that this system is not used anywhere now a days.

****QUESTION:** What is Gray Code and how do we write them?

****ANSWER:** Gray Code is a binary sequence with the property that an ordering of 2^n binary numbers such that only one bit changes from one entry to the next. Gray codes are useful in mechanical encoders since a slight change in location only affects one bit. Using a typical binary code, up to n bits could change, and slight misalignments between reading elements could cause wildly incorrect readings.

It is a number code where consecutive numbers are represented by binary patterns that differ in one bit position only.

Here you can see , for each number, there is a difference of 1 (addition or elimination of 1)

0000 =0
0001 =1
0011 =2 ,1 is added
0010 =3 , again change of 1, elimination of 1
0110 =4 ,addition of 1
0111 =5 ,again addition of 1
0101 =6 ,elimination of 1
0100 =7 ,elimination of 1
1100 =8 ,addition of 1
1101 =9 ,addition of 1

One way to construct a Gray code for n bits is to take a Gray code for n-1 bits with each code prefixed by 0 (for the first half of the code) and append the n-1 Gray code reversed with each code prefixed by 1 (for the second half). This is called a "binary-reflected Gray code". Here is an example of creating a 3-bit Gray code from a 2-bit Gray code. 00 01 11 10

A Gray code for 2 bits

000 001 011 010 the 2-bit code with "0" prefixes

10 11 01 00 the 2-bit code in reverse order

110 111 101 100 the reversed code with "1" prefixes

000 001 011 010 110 111 101 100 A Gray code for 3 bits

****QUESTION:** Explain the truth table and timing diagram of Gated S-R latch and Gated D latch in detail.

****ANSWER:** The logic symbol for the S-R flip-flop is shown here and its operation outlined in Table below.

Now we examine the output waveforms from the S-R flip-flop given the inputs. Assume that Q is HIGH initially.

The logic symbol for the D flip-flop is also shown below and its operation outlined in the Table. Notice that this flip-flop only has one input in addition to the clock called the D-input. Note that whatever is on the D-input when the trigger occurs is output at Q.

Notice that a D flip flop can be made from a S-R flip flop by ensuring that the S and R outputs are the complement of each other at all times.

****QUESTION:** How many outputs and inputs GAL22V10 have?

****ANSWER:** The GAL22V10 has 22 inputs and 10 outputs.

****QUESTION:** Explain S-R Latch? what do you mean by bistable devices?

****ANSWER:** A bistable multivibrator has two stable states, as indicated by the prefix bi in its name. Typically, one state is referred to as set and the other as reset. The simplest bistable device, therefore, is known as a set-reset, or S-R, latch.

The Q and not-Q outputs are supposed to be in opposite states. I say "supposed to" because making both the S and R inputs equal to 1 results in both Q and not-Q being 0.

For this reason, having both S and R equal to 1 is called an invalid or illegal state for the S-R multivibrator. Otherwise, making $S=1$ and $R=0$ "sets" the multivibrator so that $Q=1$ and $\text{not-}Q=0$. Conversely, making $R=1$ and $S=0$ "resets" the multivibrator in the opposite state. When S and R are both equal to 0, the multivibrator's outputs "latch" in their prior states.

By definition, a condition of $Q=1$ and $\text{not-}Q=0$ is set. A condition of $Q=0$ and $\text{not-}Q=1$ is reset. These terms are universal in describing the output states of any multivibrator circuit. So A bistable multivibrator is one with two stable output states. In a bistable multivibrator, the condition of $Q=1$ and $\text{not-}Q=0$ is defined as set. A condition of $Q=0$ and $\text{not-}Q=1$ is conversely defined as reset. If Q and not-Q happen to be forced to the same state (both 0 or both 1), that state is referred to as invalid. In an S-R latch, activation of the S input sets the circuit, while activation of the R input resets the circuit. If both S and R inputs are activated simultaneously, the circuit will be in an invalid condition. A race condition is a state in a sequential system where two mutually-exclusive events are simultaneously initiated by a single cause.

****QUESTION:** What is meant by triggering or triggering edge of clock pulse and synchronous? also what is triggering transition of clock?

****ANSWER:** Generally the term 'synchronous' means "Moving or changing at the same time". In our scenario this term also holds the same meaning. Here the two things which will change at the same time will be "Clock (CLK or C)" and the "output of the device". Means changes in the output occur with synchronization with clock.

Edge-Triggered devices change states either at the positive edge (rising edge) or the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at these two (negative or positive) edges, which in technical terms is called 'Transition of the clock'.

By examining the picture below you will understand it completely.

****QUESTION:** How to up and down the clock in J K flops plz explain the example?

****ANSWER:** In J-K flip-flops the clock moves normally as in other cases no difference. The clock pulse will change its state after the specified intervals (usually defined in 'nano seconds'(ns)) to either UP i.e '1' or DOWN i.e '0'.

****QUESTION:** what are PLD's? How are they classified.

****ANSWER:** The programmable logic devices (PLD's) are used in a lot of applications, and replace SSI and MSI circuits, due to the space saving and reduce the number of devices in a certain design. A PLD is made of a matrix of AND and OR gates, that can be programmed to obtain certain logic functions. There are four types of devices that can be classified as PLD's: a) The Programmable Read-Only Memory, PROM. b) The Programmable Logic Array, PLA. c) The Programmable Array Logic, PAL. d) The

Generic Array Logic, GAL.

****QUESTION:** What are Flip-flops?

****ANSWER:** The memory elements in a sequential circuit are called flip-flops. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit.

****QUESTION:** If an S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, then what the latch will be?

****ANSWER:** The latch will be in reset condition.

****QUESTION:** In a 4-bit Johnson counter sequence there are a total of how many states, or bit patterns?

****ANSWER:** 8