CS401 GRAND QUIZ SOLUTION BY MCS of Virtuallians

1. The base pointer accesses local variables using _____ offsets.

   Negative

2. Which of the following describes the purpose of MOVS instruction?

   Move memory to memory

3. Which part of this (0000000B80500) encoded instruction is an offset?

   0500

4. Stack is a data structure that behaves a first in last _____ manner.

   Out

5. In the instruction “mov word [es:160], 0x1230”, 30 represents _____ character.

   0

6. Multiplying two 4 bit numbers result in a _____ bit number.

   8

7. In case of near jump, the relative address is stored in _____ bits.

   16

8. _____ instructions have two parameters, one is the general purpose register to be loaded and the other is the memory location from which to load these registers.

   LDS

9. Physical memory address is of

   20 bits

10. _____ ports which interface the processor to the external world, including keyboards, mice, monitors, disc drives.

    Input, output

11. In base+offset addressing, the value contained in the base register is add with offset to get _____.

    Effective address

12. In 8051, there is an _____ stack.

    Incrementing

13. AX register can be divided into _____ and _____ bytes

Lower, higher

14. CLI stands for

Clear the interrupt flag

15. When a 32 bit number is divided by a 16 bit number, the remainder is of

16 bits

16. MUL instruction performs an unsigned multiplication of _____ with the source operand.

Accumulator

17. DW can store _____ bit value in it.

16

18. When the stack pointer, points to the return address?

When the bubble sort subroutine is called

19. IAPX88 stands for _____.

Intel Advanced Processor Extensions 88

20. 90 is the op-code of

Do nothing

21. When characters are stored in any high level or low level language, the actual thing stored in a byte is their _____.

ASCII code

22. We can convert any digit to _____ by adding 0x30 in the digit.

ASCII

23. A complete _____ is called a pass over the array

Iteration

24. Which of the following is a non-destructive AND operation?

Test

25. In _____ operation the carry flag is inserted from the right causing every bit to move one location to its left and the most significant bit occupying the carry flag.

Rotate Through Carry Left (RCL)

26. ASCII table is the contiguous arrangement of the uppercase alphabets (41-5A), the lowercase alphabets (61-7A), and the numbers _____.

    30-39

27. _____ can also be used as a masking operation to invert selective bits.

    XOR

28. BH register is a _____ bit register.

    8

29. Which of the following is the renamed version of conditional jump JZ?

    JE

30. SP is associated (by default) with _____.

    SS

31. The maximum amount of memory accessible using 8085 processor is _____.

    64 KB

32. In XOR operation the output is 1 if

    Both inputs are different

33. The clear screen operation initializes whole block of video memory to:

    0720

34. The 8088 processor divides interrupts into _____ classes.

    Two

35. Which of the following directive is used to reserve a 8 bit space in the memory for holding data?

    db

36. All mathematical and logical operations are performed on the _____

    Accumulator

37. _____ jump is not position relative but is absolute

    Far

38. Which of the following bit that “Shift Logical Right” operation copies in the carry flag?

Right most bit

39. Which of the following register is used to hold address of the next instruction to be executed?

Program counter

40. Group of bits processor uses to inform memory which element to read/write is collectively known as

Address bus

41. _____ containing the address of the next instruction to be executed.

Instruction pointer (IP)

42. To convert the case of a character, we add or subtract _____ from its ASCII code.

0x20

43. Which of the following instruction is effectively same as to multiply the value of AX by 8?

SHL AX, 8

44. _____ interrupts are those which occur side by side with some other activity.

Synchronous

45. During CALL operation, the current value of the _____ is automatically saved on the stack, and the destination of CALL is loaded in the instruction pointer.

Instruction pointer

46. In SCAS Example, we use SCASB with _____ and a zero in AL register to find a zero byte in a string

REPNE

47. In interrupt vector table. Introducing a new entry in this mapping table is called _____ an interrupt.

Hooking

48. What does the following instruction do?
ADD AX. BX

Add both registers and load value into ax register

49. The process through which the segment register can be explicitly specified as known as

Segment addressing

50. REPE and REPNE prefixes are only meaningful with _____.

CMPS

51. _____ refers to the total number of bits in a memory cell.

Cell width

52. The _____ operation is about shifting every bit one place to the right with a copy of the most significant bit left at the most significant place. The bit dropped from the right is caught in the carry basket.

Shift Arithmetic Right (SAR)

53. _____ and _____ cannot be used as 8bit register pairs like AX, BX, CX, and DX.

SI, DI

54. AX and BX both are 16-bit register, if we perform AND operation on these two registers, then how many AND operations will be performed?

16 And operation

55. 8085 can access up to _____ of memory, whereas 8088 can access up to _____ of memory.

64Kb, 1Mb

56. CS and IP are both _____ bit registers.

16

57. In 8080, there is a _____ stack.

Decrementing

58. An important role of the stack is in the creation of ____variables that are only needed while the subroutine is in execution and not afterward.

Local

59. ____ movement of data is not allowed in assembly language.

Memory-to-Memory

60. With the execution of CALL instruction, the value of____ is decremented by 2.

SP

61. In interrupt vector table, introducing a new entry in the mapping table is called____ an interrupt.

Hocking

62. Which of the following is the most illegal instruction?
    Mov al,[num 1]
63. Motorola follows____
    Big endian
64. Which of the following instruction allows code reusability in 8088?
    CALL
65. When the first thing popped off from the stack, the stack would be the return "address" and not the ____
    Argument
66. ___ decrements SP (the stack pointer) by two and then transfers a word from source operand to the top of stack now pointed to by SP,
    PUSH
67. Which of the following is a Program Control Instruction?
    cmp ax,0
68. Logical addressing is a mechanism to access ___ memory.
    Physical memory
69. In assembly language "JN2" is used to
    Jump if the zero flag is not set
70. In segmented memory model, the size of one window is restricted to _____.
    64 KB
71. Twenty-bit register is formed by the combination of two ___ bit register.
    Sixteen
72. MOV[BX+SI+300],AX is a _____ addressing mode instruction.
    Base + index + offset
73. Physical address calculating depends on
    Effective address
74. There are ____ registers in iAPX88 architecture that can hold address of data.
    4
75. ____ also known as source operand since the data is moving to stack from this operand.
    PUSH
76. By default CS is associated with
    IP
77. The stack pointer contains the address of the word that is currently on _____.
    Top the stack
78. If AX=OOFF, then which of the following instruction can be used to change the value of AX to FFOO
    ANDAX, FFOO
79. All addressing mechanisms in iAPX88 return a number called ___ address.
    Effective
80. In 8088 processor, interrupts are divided into the following classes.
    Software Interrupts, Hardware Interrupts

81. Which of the following is the interrupt number for NMI?
    INT 3
82. There are ___ registers in IAPX88 architecture that can hold address of data.
    4
83. Use of AND operation to make selective bits zero in its destination operand is known as_____.
    Selective Bit Clearing
84. Standard ASCII has ____ characters?
    128
85. ____ is used to store both the instructions to be executes by the microprocessor and the data to be used in the computation.
    Microprocessor
86. Number of operands of ADC (add with carry) register are:
    3
87. DX play an important role in arithmetic Addition.
88. Stack is a Data Structure
89. REPE or REPNE are used with the SCAS instructions
90. LDS instruction have two parameters, one is the general purpose register to be loaded and other is the memory location from which to load these registers
91. Keywords used to define two bytes program DW
92. The shift logical left operation is the exact opposite of shift logical right
93. Sending the appropriate signal on the control bus to the memory is the responsibility of Control Bus
94. A parallel port has 2 views
95. The mechanism used to drop carry for making the calculated address valid is known is address wraparound
96. In Both SHL and SAL, a zero is inserted form right and every bit moves one position to its left wth most significant but dropping in to carry flag
97. The reduction in code size and the improvement in speed are the two reasons why block processing instruction were introduced in the 8080 Processor
98. Mov ax, [NUM1] is a 16 bit move instruction
99. Which of the following is the interrupt number for debug interrupt, INT 3
100. Each entry of the interrupt vector table is of 4 bytes
101. If BL contains 000000101 then after a Singe Right Shift, BL will contain 00000010
102. AND can be used to check weather particular bit of number are set or not
103. When the relative address stored with the instruction is in 16 bit , the jump is called a Near jump
104. The Stack of 8088 works on Word Sized element
105. The interrupt call loads new values in Flag segment
106. Mov AX, 0XB800, Move ES, AX : this instruction points ES to Video Base

107. When the operant of DIV instruction is of 16 bits then implied dividend will be of 8 bits
108. Which bit is attribute but representing the blue component of foreground color 0
109. When the operand of DIV instruction is of 16-bits then implied dividend will be stored in AX Register
110. Constant can never be used as destination
111. DB-25 is a Parallel Port Connector
112. Flag register is a special register in every architecture ,, is as also known as Program Status Word
113. BP stands for base pointer
114. Intel follows little endian
115. Mov [1234].ax is an example of **direct addressing**
116. **OR** is used to clear any specific bit in a binary number
117. In general the memory cell cannot be wider than the width of the data bus.
118. mov [bx], ax moves the two byte contents of the AX register to the address contained in the BX register in the current data segment
119. source operand always resided in accumulator register
120. INT instruction takes 1 byte argument varying from 0-255.
121. Program consists of 3 logical parts
122. 8088 provides a mechanism for mapping interrupts to interrupt handlers is called hooking an interrupt.
123. The routine that executes in response to an INT instruction is called the interrupt service routine (ISR) or the interrupt handler.
124. The push operation copies its operand on the stack , while the pop operation makes a copy from the top of the stack into its operand.
125. ROR : in the rotate right operation every bit moves one position to the right and the bit dropped from the right is inserted at the left and also copied into the carry flag.
126. The segment, offset pair is called a logical address
127. the **local variables** and the **parameters** are always stored in stack segment
128. SCAS compares a source byte or word in register AL or AX with the destination string element addressed by ES:DI and updates the flags.
129. JNP and JPO is taken if the last arithmetic operation produced a number in its destination that has
odd parity
130. JP and JPE is taken if the last arithmetic operation produced a number in its destination that has
even parity.

131. There are two forms of the DIV instruction.
132. Unconditional jump always transfer the control
133. The group of bits that the processor uses to inform the memory about which element to read or write is collectively known as the **address bus.**
134. ADC has three operands
135. In direct addressing the memory address given in the instruction is **fixed**
136. In which of the following addressing, the memory address is fixed and is given in the instruction? Direct
137. **DI and SI** pair of registers used to access memory
138. Total number of cells is called the **depth**
139. **Shift Logical Right (SHR)** copies the **right most bit** in the carry flag
140. REP with **MOVS** will utilize the full processor power to do the scrolling in minimum time.
141. The correlation process from the interrupt number to the interrupt handler uses a table called **interrupt vector table**
142. POP is also known as **destination operand**
143. The **parallel** port connector is a 25pin connector called **DB-25**
144. There are just **5** block processing instructions in 8088.
145. Interrupts are **asynchronous** and unpredictable
146. **CALL** instruction allows code reusability in 8088
147. Program Control Instructions

cmp ax, 0

148. In MULTIPLICATION ALGORITHM ,We take the first digit of the multiplier and multiply it with the **multiplicand**
149. Intel CPUs are **little-endian**

while **Motorola** 680x0 CPUs are **big-endian.**

150. **JO** jump is taken if the last arithmetic operation changed the sign unexpectedly.
151. **CLI** is a special instructions
152. the interrupt call loads new values in CS
153. A 32bit processor has an accumulator of 32 bits.
154. Left shift on hexa-decimal number 9C40 ans is 0x13880
155. Each entry of the table is of four bytes
156. **VGA**. Video Graphics Adapter
157. The instruction “mov [bp], al” moves the one byte content of the AL register to the address contained in the BP register in the current **stack segment.**
158. STI stands for Set Interrupt Flag
159. Flags register is a special register in every architecture, it is also known as **program status word**

160. A special register exists in every processor called the **program counter or the instruction pointer**

161. mov word [es:160], 0x1230 12 meaning green color on blue background.

162. **DW** can store 16 bits

163. two variants of STOS are STOSB and STOSW

164. Another important role of the stack is in the creation of **local variables** that are only needed while the subroutine is in execution and not afterwards.

165. The interrupt call loads new values in CS, IP, and FLAGS.