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CS501 Solved Grand Quiz 2020

Question No 1

_____ control signal enables the input to the PC for receiving a value that is currently on the internal processor bus.

Select Correct Option

- ☒ **LPC**(For More Visit VUStudents.pk)
- ☐ INC4
- ☐ LC
- ☐ Cout

Question No 2

The Memory Buffer Register (MBR) has a _____ connection with both the memory sub-system and the registers/ALSU.

Select Correct Option

- ☐ Zero-directional
- ☐ Uni-directional
- ☒ **Bi-directional**(For More Visit VUStudents.pk)
- ☐ Tri-directional

Question No 3

MC68000 has a 32-bit program counter but only the least significant _____ bits are used.

Select Correct Option

- ☐ 8
- ☒ **16**(For More Visit VUStudents.pk)
- ☐ 20
- ☐ 24

Question No 4

All of the below given processors employ Little-Endian storage format expect_____.

Select Correct Option

- ☐ EAGLE
- ☐ Modified EAGLE
- ☒ **Falcon-A**(For More Visit VUStudents.pk)
- ☐ Falcon-E



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Question No 5

While executing the RTL instruction $A \leftarrow R3$. Which of the given below control signals will be activated?

Select Correct Option

- ✓ **LA, R3in**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ R3out
- ✓ LA, R3out
- ✓ R3in, Lout

Question No 6

Which of the following RTL descriptions is used to represent the target of Falcon-A instruction?

Select Correct Option

- ✓ $rb<2..0> := IR<7..5>$
- ✓ $ra<2..0> := IR<10..8>$
- ✓ **$rb<2..0> := IR<10..8>$**([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ $rc<2..0> := IR<4..2>$

Question No 7

Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

Select Correct Option

- ✓ Instruction Register
- ✓ Memory Address register
- ✓ Memory Buffer Register
- ✓ **Registers A and C**.....([For More Visit VUStudents.pk](http://VUStudents.pk))

Question No 8

Which of the following register is used as an implicit operand in MUL/DIV instruction of Falcon-A?

Select Correct Option

- ✓ R0
- ✓ OC
- ✓ **IR**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ SP





Question No 9

In Which of the following addressing modes, the address of the memory from where the value is to be accessed is given in the instruction?

Select Correct Option

- ✓ **Direct Addressing**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ Immediate Addressing
- ✓ Indirect Addressing
- ✓ Register Direct Addressing

Question No 10

Which one of the following control signals causes the data from the bus to be read into the register MAR.

Select Correct Option

- ✓ MARout
- ✓ MARin
- ✓ **LMAR**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ None of the given

Question No 11

Program counter (PC) and Instruction register (IR) are normally 16-bit registers, however in SRC, these are _____.

Select Correct Option

- ✓ 31-bit
- ✓ 16-bit
- ✓ **32-bit**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ 64-bit

Question No 12

_____ controls the sequence of the flow of microinstructions.

Select Correct Option

- ✓ Multiplexer
- ✓ **Micro Program controller**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ DMA Controller
- ✓ Virtual memory





Question No 13

The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by_____.

Select Correct Option

- ✓ **Data forwarding**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ Data compressing
- ✓ Instruction forwarding
- ✓ Instruction handling

Question No 14

All registers of FALCON-A are of _____ while in case of SRC all registers are _____.

Select Correct Option

- ✓ **16-bits, 32 bits**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ 24-bits, 32 bits
- ✓ 32-bits, 16 bits
- ✓ 32-bits, 64 bits

Question No 15

Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Select Correct Option

- ✓ Arithmetic
- ✓ Control
- ✓ **Data transfer**.....([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ Floating point

Question No 16

In SRC, which of the following notation which is used to represent 32-bit memory word stored at address starting from 56?

Select Correct Option

- ✓ $M[56]<31..0> := M[56] M[57] M[58] M[59]$
- ✓ **$M[56]<0..31> := M[56] M[57] M[58] M[59]$**([For More Visit VUStudents.pk](http://VUStudents.pk))
- ✓ $M[56]<0..31> := M[59] M[58] M[57] M[56]$
- ✓ $M[56]<31..0> := M[59] M[58] M[57] M[56]$





Question No 17

A machine cycle is defined to be the time it takes to fetch _____ operands from registers, perform an Arithmetic Logic Unit (ALU) operation and store the result in a register.

Select Correct Option

- ✓ **Three**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ Two
- ✓ One
- ✓ Four

Question No 18

In a processor, _____ is responsible for the synchronization of internal as well as external events.

Select Correct Option

- ✓ Memory Unit
- ✓ Data Unit
- ✓ **Arithmetic & Logical Unit**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ Control Unit

Question No 19

For a processor having 32 general purpose registers, _____ bits are required for each register field in the instruction.

Select Correct Option

- ✓ **32**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ 3
- ✓ 8
- ✓ 5

Question No 20

Which temporary register is loaded with either a register value file or a constant from the instruction?

Select Correct Option

- ✓ **Y3**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ X3
- ✓ Z4
- ✓ Z5





Question No 21

_____ provides a temporary storage for the address of memory location to be accessed.

Select Correct Option

- ☒ **MAR**.....(For More Visit VUStudents.pk)
- ☐ MBR
- ☐ PC
- ☐ LPC

Question No 22

What does the word 'D' in the D-flip-flop' stand for?

Select Correct Option

- ☒ **Data**.....(For More Visit VUStudents.pk)
- ☐ Digital
- ☐ Dynamic
- ☐ Double

Question No 23

The syntax of the instruction "branch and link if zero" is

Select Correct Option

- ☐ brzr ra, rb, rb
- ☐ brnz ra, rb, rc
- ☒ **brlzl ra, rb, rc**.....(For More Visit VUStudents.pk)
- ☐ brlnz ra, rb, rc

Question No 24

In SRC, the effective address is computed at run-time by adding a constant to value of ____ register.

Select Correct Option

- ☐ FLAGS
- ☐ IR
- ☒ **PC**.....(For More Visit VUStudents.pk)
- ☐ RA





Question No 25

To apply two shifts to an input number using the barrel shifter, the control signals S1 and S0 of the shifter should be _____.

Select Correct Option

- ✓ **S1 = 1 and S0 = 1**(For More Visit VUStudents.pk)
- ✓ S1 = 0 and S0 = 1
- ✓ S1 = 1 and S0 = 0
- ✓ S1 = 2 and S0 = 0

Question No 26

In MC68000, _____ register is used as stack pointer.

Select Correct Option

- ✓ **A0**(For More Visit VUStudents.pk)
- ✓ A7
- ✓ D0
- ✓ D7

Question No 27

In the case of a constant, variable, an address or (label-PC), the unconditional jump ranges _____.

Select Correct Option

- ✓ **From -128 to 127**(For More Visit VUStudents.pk)
- ✓ From -64 to 63
- ✓ From -256 to 255
- ✓ From -32768 to 32767

Question No 28

The SPARC architecture defines a _____ that allows for multiple address spaces.

Select Correct Option

- ✓ **Memory Logic Unit (MLU)**(For More Visit VUStudents.pk)
- ✓ Memory Mapping Unit (MMU)
- ✓ Memory Shifting Unit (MSU)
- ✓ Memory Arithmetic Unit (MAU)





Question No 29

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory.

Select Correct Option

- ✓ Jump
- ✓ Control
- ✓ **Load/store**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ Branch

Question No 30

RISC stands for?

Select Correct Option

- ✓ Registers internal system cache
- ✓ **Reduced instruction set computer**.....([For More Visit VUStudents.pk](https://VUStudents.pk))
- ✓ Register instruction set computer
- ✓ Reduced internal system computers

THE END

