CS501 – Advance Computer Architecture

Grand Quiz December 2020

Prepared By: MCS of Virtuallians

If fount any error please correct it accordingly

1. Execution time of a program with respect to the processor is calculated as:
   a. Execution Time = IC x CPI x MIPS
   b. Execution Time = IC x CPI x T page 42
   c. Execution Time = CPL x T x MFLOPS
   d. Execution Time = ICxT
2. Which one of the followings is the correct RTL description for sign extension of an 8-bit constant?
   a. (8αlR<7>©IR<7.0>) page 148
   b. (8αlR<8> ©IR<8.. 1>)
   c. (8αlR<7> ©IR<8.0>)
   d. (8αlR<8>©R<7.. 0>)
3. Which of the following conditions is evaluated when executing the branch instruction "brzr R2, R1"?
   a. if (R2 == 0)
   b. if (R1 > 0)
   c. if (R1 == 0) page 153
   d. if (R1 <0)
4. An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a:
   a. compiler
   b. cross assembler page 24
   c. debugger
   d. linker
5. Which of the following is NOT related to the architecture of a computer?
   a. Instruction set
   b. Control signals page 19
   c. 1/O mechanisms
   d. Memory addressing modes
6. Which of the following register holds the address of next instruction to be executed?
   a. Accumulator Register
   b. Instruction Register
   c. Program Counter page 25
   d. Base Register

7. In Type C instruction of SRC, the maximum size of constant field is_____ bits.
    a. 8
    b. 16
    c. 17 page 46
    d. 27
8. Among the two approaches available to design a control unit, hardwired approach is relatively _____as compared to micro-programming
    a. Slow
    b. Average
    c. Faster page 171
    d. Better
9. All of the below given processors employ Little-Endian storage format except_____
    a. EAGLE
    b. Modified EAGLE
    c. Falcon-A
    d. Falcon-E
10. Which of the following measures can be best used for calculating the performance of computation intensive applications?
    a. MIPS
    b. MFLOPS page 43
    c. Whetstones
    d. Dhrystones
11. RISC stands for?
    a. Registers internal system cache
    b. Reduced Instruction Set Computer page 20
    c. Register Instruction Set Computer
    d. Reduced Internal System Computers
12. Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
    a. Accumulator
    b. Address Mask
    c. Instruction Register
    d. Program Counter
13. In FALCON A Program Counter (PC) and Instruction Register (IR) are of _____bits
    a. 16-bits page 88
    b. 24-bits
    c. 32-bits
    d. 64-bits

14. In FALCON-A processor, memory word size is
    a. 1 byte
    b. 4 bytes
    c. 2 bytes page 88
    d. 8 bytes

15. To set the value of micro-PC from branch address, the value of 4 to 1 multiplexer is_____
    a. 00
    b. 01
    c. 10
    d. 11 page 209

16. Type checking allows the _____ to determine memory requirements for variables.
    a. Compiler page 25
    b. Debugger
    c. Linker
    d. Loader
17. In MC68000, only the last_____ bits of 32-bit program counter (PC) register are used to store memory addresses.

    a. 8
    b. 16
    c. 24
    d. 32
18. What is the instruction length of the FALCON-E processor?
    a. 8 bits
    b. 16 bits
    c. 32 bits page 119
    d. 64 bits

19. RTL statements separated by____ are always executed in same clock pulse.
    a. Colon (;)
    b. Comma(,) page 66
    c. Semi-colon (:)
    d. Hash (#)
20. mul is the example of a(n) _____operation

    a. Logic
    b. Shift
    c. Arithmetic
    d. Data transfer

21. Which of the following control signals is NOT activated during instruction fetch operation?
    a. PCout
    b. LC
    c. LMAR
    d. Cout
22. The size of data bus of MC68000 processor is
    a. 8 bits
    b. 16 bits
    c. 20 bits
    d. 32 bits
23. A collection of ----------is called a micro program.
    a. large scale operations
    b. Registers
    c. DMA
    d. Microinstructions page 205
24. In SRC, the general-purpose register file includes ____ registers each 32 bit wide.
    a. 16 registers RO to R15
    b. 24 registers RO to R23
    c. 32 registers RO to R31 page 140
    d. 64 registers RO to R63
25. Which of the following RTL descriptions is used for specifying theoperation of an SRC instruction?
    a. IR<31..27> pg 65
    b. IR<22..26>
    c. IR<21..17>
    d. IR<21..0>
26. The instruction "PUSH A" is an example of_____
    a. 0-address instruction
    b. 1-address instruction
    c. 2-address instruction
    d. 3-address instruction
27. To implement an N-bit barrel shifter in form of a combinational circuit, we require N_____
    a. Multiplexers pg 81
    b. demultiplexers
    c. selectors
    d. tri-state buffers

28. A general purpose digital computer has_____ components.
    a. 2
    b. 3 Pg 18
    c. 4
    d. 5
29. _____form the branch control field in the micro instruction.
    a. C Bits
    b. M Bits
    c. B Bits pg 206
    d. A Bits
30. The third stage of the Pipelined version of SRC is;
    a. Instruction Fetch
    b. ALU operation pg 190
    c. Memory access
    d. Register write
31. The instruction "Shiftl R1, R2, 20" is an example of which of thefollowing addressing modes?
    a. Relative
    b. Displacement
    c. Register
    d. Immediate pg 98
32. In pipe-lined processors, there should be a _____port register file so that if the register write and register read stages overlap, they can be performed in parallel.
    a. Four
    b. Three pg 188
    c. Two
    d. One
33. For any of the instructions that are a part of the instruction set of the SRC, there are certain _____required; which may be used to Select the appropriate function for the ALU to be performed, to
    Select the appropriate registers, or the appropriate memory location.
    a. Registers
    b. Control signals pg 158
    c. Memory
    d. None of the given
34. Which one of the following control signals allow the value of registers rc to be read?
    a. RCE pg 170
    b. RBE
    c. LCON
    d. RCON

35. in a _____the address of next instruction to be executed is also given with the current instruction.
    a. 1-address instruction
    b. 2-address instruction
    c. 3-address instruction
    d. 4-address instruction page 32
36. Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
    a. Instruction Register
    b. Memory address register
    c. Memory Buffer Register
    d. Registers A and C pg 140
37. Which of the following RTL descriptions is used to represent allgeneral purpose registers of SRC?
    a. R [1..32]<32..1>;
    b. R [1..32]<31..>;
    c. R (0..31]<32..1>;
    d. R (0..31]<31..>; pg 65
38. _____is the highest level of digital design abstraction in which computer architect views the system for the description of system components and their interconnections.
    a. Processor Memory Switch level pg 20
    b. Instruction Set Level
    c. Register Transfer Level
    d. Control Tranfer Level
39. Which of the given below measure(s) is/are used for comparison of performance of various machines?
    a. Execution time
    b. MFLOPS
    c. MIPS
    d. All of the given pg 42
40. _____is an example of miscellaneous instruction.
    a. Shift
    b. Store
    c. Halt pg 70,86
    d. Call

41. Which of the given RTL descriptions is used to represent "load register relative (Idr)" instruction?
    a. (op<4..O>= 6): R (ra) - rel
    b. (op<4..0>= 2): R (ra) - M [rel] pg 68
    c. (op=4..0>= 3): M (disp) - R [ra]
    d. (op=4..0>= 4): M[rel] - R[ra]
42. What functionality is performed by the instruction "lar R3, 36" of SRC?
    a. It will load the register R3 with the contents of the memory location OM (PC+36]
    b. It will load the register R3 with the relative address itself (PC+36). pg 46
    c. It will store the register R3 contents to the memory location MO [PC+36]
    d. It will left rotate the value of R3, 36 times and will store the result o into R3
43. There are types of reset operations in SRC.
    a. Three
    b. Four
    c. Two pg 179
    d. Five
44. What is the size of the memory space that is available to FALCON-A processor?
    a. 2^8 bytes
    b. 2^16 bytes
    c. 2^32 bytes
    d. 2^64 bytes
45. Which of the following registers is used as an implicit operand in MUL/DIV instruction of Falcon-A?
    a. RO page 92
    b. PC
    c. IR
    d. SP
46. A relative address is calculated by adding the displacement to the contents of the_____
    a. Program Counter pg 103, 62
    b. Instruction Register
    c. General Purpose Register
    d. Flags Register

47. Which of the given below measure(s) is/are used for comparison of performance of various machines?
    a. Execution time
    b. MFLOPS
    c. MIPS
    d. All of the given pg 42

48. Which of the followings is a behavioral RTL description to enable the exceptions?
    a. IE 0
    b. IE – 1 pg 184
    c. IE --1
    d. IE 8

49. All of the given are examples of register-to-memory data transfer instructions except
    a. Idacc
    b. Id
    c. st
    d. Lar pg 128

50. _____Control signal enables the input to the PC for receiving a value that is currently on the internal processor bus.
    a. LPC page 159
    b. INC4
    c. LC
    d. Cout

51. Below given RTL description belongs to which stage of pipe-lining?
    IR2 – M[PC]
    PC2-PC+4;
    a. Instruction Fetch pg 196
    b. Instruction Decode
    c. Memory Access
    d. ALU Operation

52. Control signal for RTL "R<-MBR" will be_____
    a. MBRout. LIR page 179
    b. PC <--C
    c. PC<--MBR
    d. PC<--IR

53. Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
    a. := pg 64
    b. &
    c. %
    d. ©

54. In EAGLE processor, the displacement size for both conditional and unconditional is_____
    a. 16 bits
    b. 32 bits
    c. 8 bits pg 130
    d. 27 bits
55. Which of the followings is not an example of super-scalar processors?
    a. PowerPC 601
    b. IAPX88 pg 204
    c. Intel P6
    d. DEC Alpha 21164
56. The instruction "Load R1. [R3 + 20]" is an example of which of the following addressing modes?
    a. Direct
    b. Immediate
    c. Register
    d. Displacement pg 98
57. The multiplexer_____is used to decide which value is transferred to be written back to the register file.
    a. MP2
    b. MP3
    c. MP4
    d. MP5 pg 195
58. Which of the following notations represents the indexed or scaled addressing mode in any processor?
    a. [[R4]+[R5]] pg 130
    b. M[R1+25]
    c. M[R2].
    d. [123]
59. Which of the following bits of SRC instruction are used as short displacement or to specify an immediate operand?
    a. c2<11..0> = IR<11..>;
    b. c2<21.0>:= IR<21..0>
    c. c2<16.0>:= IR<16.0>: pg 65
    d. c2<11..0> = IR<11..0>:
60. To connect together N registers in a point to point scheme, we require_____ connections
    a. N(N+1)
    b. N(N-1) pg 79
    c. 2N
    d. 2N(N-1)

61. Which one of the following is a bi-stable device, capable of storing one bit of Information?
    a. Decoder
    b. Flip-flop pg 74
    c. Multiplexer
    d. Diplexer
62. Which one of the following operations is NOT performed by using miscellaneous instructions?
    a. Clearing all registers
    b. Stopping the processor
    c. NOP
    d. Returning from a procedure
63. "If P = 1, then load the contents of register R1 into register R2". This statement can be written in RTL as:
    a. R1 <-R2
    b. P:R1 <-R2
    c. P: R2<-R1
    d. P: R2<-R1. P: R1 <-R2
64. In the case of a constant, variable, an address or (label-PC), the unconditional jump ranges
    a. from-128 to 127 pg 150
    b. from -64 to 63
    c. from-256 to 255
    d. from -32768 to 32767
65. Which of the following is NOT an advantage of using register-to-register data transfers
    a. It is simpler
    b. It is faster
    c. It is most compact page 128
    d. It is easier to pipeline
66. In EAGLE processor, which of the following notations is used to represent a memory word stored at address 8?
    a. M[8]<0...15> :=M [8] ©M[9]
    b. M[8]<15.0>:= M [9] ©M[8] pg 113
    c. M[8]<15.0>:= M [8] ©M [9]
    d. M[8]<0.15>:= M [9]© M [8]
67. The ALSU function "INC2" increments the by 2 and the output is stored in the buffer register
    a. PC.A
    b. IR.A
    c. PC.C pg154
    d. IR.C

68. ___hazard occurs when attempting to access the same resource in different ways at the same time
    a. Branch
    b. Data
    c. Structural pg 198
    d. Instruction
69. Motorola MC68000 is an example of microprocessor
    a. CISC pg 137
    b. RISC
    c. SRC
    d. FALCON
70. In SRC. the memory is accessed in the chunks of _____ byte(s) each
    a. 2
    b. 4 pg 44
    c. 16
    d. 32
71. Which one of the following control signals causes the data from the bus to be read into the register MAR.
    a. MARout
    b. MARin
    c. LMAR pg 154
    d. None of the given
72. Pipeline hazard occurs when an instruction depends on the result of _____ instruction that is not yet complete.
    a. next
    b. previous pg 231 , 198
    c. ongoing
    d. first
73. Which one of the followings is the correct RTL description for sign extension of a 5-bit constant?
    a. 5αIR<4> ©IR<4.0>
    b. 5αIR<5>© IR<5.. 1>)
    c. 11αIR<4> ©IR<4..0>) page 148
    d. 11αIR<4>© IR<5.. 1>)
74. In Falcon-A processor, first 5 most significant bits from the IR are fed to a_____ decoder.
    a. 5-to-32 pg 173
    b. 5-to-10
    c. 5-to-31
    d. 11-to-15

75. "Finite-state machine" concepts are usually used to represent the Control Unit where every state corresponds to clock cycle(s)
    a. 1 pg 172
    b. 2
    c. 4
    d. 16

76. The status register of the 68000 has __condition codes.
    a. 2
    b. 3
    c. 5
    d. 8

77. SPEC stands for_____
    a. Scientific Performance Execution Cooperative
    b. System Performance Execution Cooperative
    c. Scientific Performance Evaluation Cooperative
    d. System Performance Evaluation Cooperative pg 36

78. Which of the following register holds the address of next instruction to be executed?
    a. Accumulator
    b. Address mask
    c. Instruction register
    d. Program Counter page 25

79. Almost every commercial computer has its own particular language
    a. Scripting Language
    b. Visual Language
    c. Higher Level Language
    d. Assembly Language

80. _____usually involves calculating the target address and evaluating a condition.
    a. Load/Store instructions
    b. Branch Instructions pg 193
    c. ALU instructions
    d. Pipelined SRC

81. If the most significant two digits of hexadecimal equivalent of an SRC instruction are "E1", the opcode of such an instruction is_____
    a. str
    b. ldr
    c. shr
    d. shl pg 54 (EI= 1110 0001, 11100 = shl)

82. A Stack based machine is also called
    a. 0-address machine page 31
    b. 1-address machine
    c. 2-address machine
    d. 3-address machine
83. In which of the following addressing modes, the address of the memory from where the value is to be accessed is given in the instruction?
    a. Direct Addressing
    b. Immediate Addressing
    c. Indirect Addressing
    d. Register Direct Addressing
84. What functionality is performed by the instruction "str R8, 34" of SRC?
    a. It will load the register R8 with the contents of the memory location M [PC+34]
    b. It will load the register R8 with the contents of the memory location M [34]
    c. It will store the register R8 contents to the memory location M [PC+34] pg 39
    d. It will store the register R8 contents to the memory location M [34]
85. In Type-1 instruction, bits____ are reserved for the op-code.
    a. bits through 8
    b. bits 1 through 5
    c. bits 0 through 4 page 90
    d. bits 11 through 15
86. From the given stages of pipelining, which one is used for loading an instruction from the memory for execution?
    a. ALU Operation
    b. Memory Access pg 216
    c. Fetch Operand
    d. Fetch Instruction
87. The_____ control signal is used to enable the tri-state buffers with the MBR
    a. LMAR
    b. LMBR
    c. MARout pg182
    d. MBRout
88. Program counter (PC) and Instruction register (IR) are normally 16-Bit registers, however in SRC. these are
    a. 31-Bit
    b. 16-Bit
    c. 32-Bit page 48
    d. 64-Bit

89. During the RESET operation of processor, control step counter is set to
    a. 0 pg 208
    b. 1
    c. 2
    d. -1
90. _____controls the sequence of the flow of Micro instructions.
    a. Multiplexer
    b. Micro program controller 239
    c. DMA Controller
    d. Virtual Memory
91. The ____control signal enables the input to the register C for writing the incremented value of PC onto it
    a. INC4
    b. LC pg 182
    c. PCout
    d. LPC
92. In RTL, which of the following symbols is used to store some data into a register?
    a. ;
    b. <-
    c. :=
    d. == loading and assigning
93. What does the word 'D' in the 'D-flip-Flop' stand for?
    a. Data google
    b. Digital
    c. Dynamic
    d. Double
94. _____ is defined as the number of instructions processed per second
    a. Memory Access
    b. Throughput page 187
    c. ALU Operations
    d. Latency
95. The MAR is connected directly to the_____
    a. MBR
    b. CPU internal bus
    c. CPU external bus page 154
    d. LIC

96. In a processor, _____is responsible for the synchronization of internal as well as external events.
    a. Memory Unit
    b. Data Unit
    c. Arithmetic & Logical Unit
    d. Control Unit page 198

97. Which one of the following registers holds the instruction that is being executed?
    a. Accumulator
    b. Address Mask
    c. Instruction Register page 155
    d. Program Counter

98. Total number of data registers in Motorola 68000 processor are_____
    a. 8 google
    b. 12
    c. 24
    d. 32

99. Which of the following types of unconditional jump is also known as near jump?
    a. Direct
    b. Register relative
    c. PC relative page 128
    d. Indirect

100. In _____only one field is required which specifies the type of operation
    a. 3-Address Instruction
    b. 2-Address Instruction
    c. 1-Address Instruction
    d. 0-Address Instruction pg 24

101. _____ operation is required to change the processor`s state to a known , defined value
    a. Update
    b. Reset page 208
    c. Halt
    d. Changes

102. Which of the following bits of SRC instruction are used to hold an operand , an address index , or a branch target register
    a. The bits 16 through 0
    b. The bits 26 through 22
    c. The bits 21 through 17 page 60
    d. The bits 17 through 0

103. The SRC uses a hazard detection unit , the hazard can be resolved using either pipeline stalls or by _____
   a. Data Forwarding page 232
   b. Data compressing
   c. Instruction forwarding
   d. Instruction handling

104. In _____instruction format of EAGLE processor there in no field reserved for operands
   a. Type V
   b. Type X
   c. Type Y
   d. Type Z

105. VLIW stand for _____
   a. Variable length instruction word
   b. Very Long instruction word
   c. Very long instruction width
   d. Variable length instruction width

106. In case of FALCON-A, _____ instructions are present which are not present in the SRC processor.
   a. Create and destroy
   b. In and out
   c. Open and close
   d. Read and write

107. Which type of instruction enables mathematical computations?
   a. Arithmetic
   b. Control
   c. Data transfer
   d. Numeric

108. CISC Stands for ?
   a. Computer instruction set compiler
   b. Complex instruction set computer
   c. Complex internal system computer
   d. Complex instruction system compiler

109. Which instruction is used to store register to memory usingrelative address?
   a. Id instruction
   b. Idr instruction
   c. lar instruction
   d. str instruction page 148

110. The _____ instruction is completed once memory access has been made and the memory location has been written to.
   a. Link
   b. Branch
   c. Store page 192
   d. Control

111. ret and jmi both belong to _____ type Instructions
   a. Arithmetic
   b. Control page 86
   c. Data Transfer
   d. Logic

112. Which of the following is example of direct indirect addressing mode?
   a. [25] direct addressing) page 130
   b. M[R6]
   c. M[R1+25]
   d. M[[R5]+[R6]]

113. A machine cycle is defined to be the time it takes to fetch _____ operands from registers perform an Arithmetic logic Unit (ALU) operation and store the result in a register.
   a. Three
   b. Two
   c. One
   d. Four

114. In the 3-bus Implementation for the SRC, all the specialpurpose as well as the general purpose registers have _____ read port(s) _____ write port(s)
   a. one, two
   b. two, one page 178
   c. two, two
   d. three, one

115. A collection of all possible machine language commands that a computer can understand and execute is called _____.
   a. Bytecodes
   b. Instruction Set page 23
   c. Mnemonics
   d. Opcodes

116. In "DIV R3" instruction of EAGLE, the register ____is used as both sources operand and destination operand
   a. R0 page 110
   b. R1
   c. R2
   d. R3

117. To apply two shots to an input number using the barrel shifter, the control signals S1 and SO of the shifter should be _____.
   a. S1 = 1 and S0 = 1
   b. S1 = 0 and S0 = 1
   c. S1 = 1 and S0 = 0 page 82
   d. S1 = 2 and S0 = 0

118. The result is stored in the destination register in _____ stage of the pipeline.
   a. Instruction fetch
   b. ALU5 operation
   c. Memory access
   d. Register write page 187

119. In any instruction, the possible locations of the source operands can be _____.
   a. CPU Registers
   b. Memory Cells
   c. I/O Locations
   d. All of the given page 31

120. The syntax of the instruction "branch and link if zero" is
   a. brzrra, rb, rc
   b. brnz ra, rb, rc
   c. brlzr ra, rb, rc page 144
   d. brlnz ra, rb, rc

121. In a Falcon-A assembly program, labels are used to implement _____ jump.
   a. Direct
   b. Indirect
   c. Relative page 92
   d. Displacement

122. All registers of FALCON-A are of _____ while in case of SRC all registers are _____.
   a. 16-bits, 32 bit page 42
   b. 24-bits, 32 bit
   c. 32-bits, 16 bit
   d. 32-bits, 64 bit

123. Which of the following RTL descriptions is used to represent the target register of Falcon A instruction?
   a. rb<2..0> := IR<7..5>:
   b. ra<2..0> := IR<10..8>: page 102
   c. rb<2..0> :=IR<10..8>:
   d. rc<2..0> := IR<4..2>:

124. jump [ra+c2] is an _____ instruction
   a. Conditional jump
   b. Unconditional jump page 150
   c. Shift
   d. Arithmetic and logic
125. MC68000 has a 32-bit program counter but only the least significant _____ bits are used.
   a. 8
   b. 16
   c. 20
   d. 24
126. The instruction fetch procedure generally takes _____ time step(s).
   a. one
   b. two
   c. three page 141
   d. four
127. For a processor having 32 general purpose registers, _____ bits are required for each register field in the instruction
   a. 32
   b. 3
   c. 8
   d. 5
128. Type D instruction format of SRC includes _____ ALU registers.
   a. 3
   b. 4
   c. 1
   d. 2
129. While executing the RTL instruction A =R3, which of the given below control signals will be activated?
   a. LA, R3in
   b. R3 out
   c. LA, R3out
   d. R3in, Lout
130. What is the working of Processor Status word (PSW)?
   a. To hold the current status of the processor
   b. To hold the address of current process
   c. To hold the instruction that the computer is currently processing
   d. To hold the address of the next instruction in memory that is to be executed

131. In a Falcon-E instruction _____ bits are reserved for opcode.

a. 3
b. 5 page 119
c. 6
d. 8